2.(Original) Storage device according to Claim 1, comprising a memory-specific logic device (L) and an interrupt line (STL) to transmit an interrupt signal (st) to a processor system (PU) so as to control the complete system such that by sending the interrupt signal (st), an interruption of the processor operation is always triggered for one clock cycle whenever a memory access is to be effected by the memory (M) to two different buses (P, D0, D1, R), or to the memory (M) by these buses, within two successive clock cycles.

3.(Currently Amended) The storage device ~~Memory~~ according to Claim 1 ~~or 2~~, comprising an analyzer (ARB, CU) connected on the input side of the memory (M) for analyzing addresses on the address lines (AL) assigned to the buses and/or the memory for memory accesses, and for appropriately switching the switching device (SW) to one of the corresponding buses (P, D0, D1, R).

4.(Original) Storage device according to Claim 3, wherein the analyzer (ARB, CU) is designed for analyzing a part of the addresses, and for switching and assigning a memory access for address segments smaller than the word width of a bus transmitting the addresses or of the address lines (AL).

5.(Currently Amended) Storage device according to Claim 3 ~~or 4~~, comprising an adjustable separator device, specifically a programmably adjustable separator device (MTR) to store a memory address of the memory (M) for analysis by the analyzer (ARB, CU).

6.(Currently Amended) Storage device according to ~~one of~~ Claims 3 ~~5~~, wherein the analyzer has a common access control device (ARB) to switch the switching device (SW), and one comparator (CU) each per bus (P, D0, D1, R) to compare the address with the memory address of the memory (M).

7.(Currently Amended) Storage device according to ~~one of~~ Claim 3 ~~6~~, wherein the analyzer has a modifier (MOD) which is designed to process different data types and/or access types which are applied to the modifier (MOD) and/or to a data memory segment of the memory (M)

through data lines, subaddress lines, and/or access signal lines (DL, SAL, ACL) selected by the switching device (SW) in order to transmit states on the bus lines (DL).

8.(Currently Amended) Storage device according to claim 7, ~~one of the foregoing claims,~~ comprising a or the logic device (L, CU) to issue a block loss signal (BM) through a loss line (BML) to a higher-level processor system (PU) in response to a deviation from the announced and executed data transfers during the memory access.

9.(Currently Amended) Storage device of claim 1, comprising a plurality of storage devices ~~according to a foregoing claim~~ which is switchably connected to one bus each within a multibus architecture having a plurality of busses (P, D0, D1, R).

10.(Original) Storage system according to Claim 9, which – particularly in the case of a switch between read access and write access for one of the memories (M) – is designed to effect the clock-cycle-based alternating control of different memories (M) by a common high-level processor system (PU).

11.(Cancelled)

12.(Cancelled)

13.(Cancelled)

14.(Cancelled)

15.(Cancelled)

16.(Cancelled)

17.(Cancelled)

18.(Cancelled)

19.(Cancelled)